Claims

[c1] A method of fabricating a thin channel silicon-on-insulator device comprising:
providing a structure including at least a substrate having a layer of semiconducting material atop an insulating layer and a gate region formed atop said layer of semiconducting material;
forming a conformal oxide film atop said structure;
implanting said conformal oxide film with a first dopant impurity to form a first dopant impurity region;
forming a set of spacers atop said conformal oxide film, said set of spacers are adjacent to said gate region;
removing portions of said conformal oxide film, not protected by said set of spacers to provide an exposed region of semiconducting material;
forming raised source/drain regions on said exposed region of said semiconducting material;
implanting said raised source/drain regions with a second dopant impurity to form a second dopant impurity region; and
activating said first dopant impurity region and said second dopant impurity region, whereby source/drain and source/drain extension regions are formed in said layer

of semiconducting material.

[c2] The method of Claim 1 wherein said layer of semiconducting material has a thickness of less than about 200 Å.

[c3] The method of Claim 1 wherein said raised source/drain regions are formed by a selective epitaxial growth process.

[c4] The method of Claim 1 wherein said epitaxial growth process comprises depositing silicon.

[c5] The method of Claim 1 wherein said conformal oxide film is formed by chemical vapor deposition (CVD), plasma-assisted CVD, high-density plasma chemical vapor deposition (HDPCVD), atomic layer deposition or thermal growth.

[c6] The method of Claim 1 wherein said conformal oxide film has a thickness ranging from about 2 nm to about 20 nm.

[c7] The method of Claim 1 wherein said portions of said conformal oxide film are removed by wet etching, dry etching, or a combination thereof.

[c8] The method of Claim 1 wherein said first dopant impurity is a group IIIA dopant or a group V dopant.

[c9] The method of Claim 1 wherein said activating said first dopant impurity region comprises an annealing process which forms said source/drain regions underlying a remaining portion of said conformal oxide film.

[c10] The method of Claim 1 wherein said second dopant impurity is a group IIIA dopant or a group V dopant.

[c11] The method of Claim 1 wherein implanting said conformal oxide film comprises an implant dose ranging from about $3x10^{13}$ atoms/cm^2 to about $3x10^{16}$ atoms/cm^2.

[c12] The method of Claim 1 wherein implanting said conformal oxide film comprises an implant energy of about 0.2 keV to about 15 keV.

[c13] The method of Claim 1 further comprising forming a second set of spacers adjacent said set of sidewall spacers prior to implanting said raised source/drain regions.

[c14] The method of Claim 1 wherein said implanting said conformal oxide film further comprises halo implants.

[c15] A method of fabricating a thin channel silicon-on-insulator device comprising:
providing a structure including at least a substrate having a layer of semiconducting material atop an insulating layer and a gate region formed atop said layer of semi-

conducting material;
forming a doped oxide film atop said structure;
forming a set of spacers atop said doped oxide film, said set of spacers are adjacent to said gate region;
removing portions of said doped oxide film, not protected by said set of spacers to provide an exposed region of semiconducting material;
forming raised source/drain regions on said exposed region of said semiconducting material;
implanting said raised source/drain regions with a dopant impurity to form a dopant impurity region; and
activating said doped oxide film and said second dopant impurity region, whereby source/drain and source/drain extension regions are formed in said layer of semiconducting material.

[c16] A thin channel silicon-on-insulator device comprising:
a substrate having a layer of semiconducting material atop an insulating layer;
a gate region atop said layer of semiconducting material;
a doped oxide film conformal to at least a sidewall of said gate region sidewall and atop a portion of said semiconducting material;
a set of spacers located on a horizontal surface of said conformal oxide film adjacent to said gate region; and
a raised source/drain region on either side of said gate

region, where said raised source/drain region are separated from said gate region by said set of spacers.

[c17] The thin channel silicon-on-insulator device of Claim 16 further comprising an extension region in said layer of semiconducting material underlying said portion of oxide film.

[c18] The thin channel silicon-on-insulator device of Claim 15 further comprising halo regions, which are located underneath and laterally adjacent to said extension regions in said channel.

[c19] The thin channel silicon-on-insulator device of Claim 15 further comprising an additional set of spacer adjacent said set of spacers.